ABSTRACT OF THE DISCLOSURE

Gate lines are formed on a substrate. A gate insulating layer, a semiconductor layer, an intrinsic a-Si layer, an extrinsic a-Si layer, a lower film of Cr and an upper film of Al containing metal are sequentially deposited, and the upper film and the lower film are patterned to form data lines and drain electrodes. A photoresist is formed, and the upper film is patterned using the photoresist as an etch mask to expose contact portions of the lower film of the drain electrodes. Exposed portions of the extrinsic a-Si layer and the intrinsic a-Si layer are removed, and then the photoresist and underlying portions of the extrinsic a-Si layer are removed. A passivation layer is formed and patterned along with the gate insulating layer to form contact holes exposing the contact portions of the lower film, and pixel electrodes are formed to contact the contact portions.